

In situ Electrical Characterization of the Thickness Dependence of Organic Field-Effect Transistors with 1–20 Molecular Monolayer of Pentacene

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ABSTRACT Field-effect mobility (μ) of pentacene-based organic field-effect transistors (OFETs) is studied as a function of the number of molecular monolayer (ML) by in situ electrical characterization, which greatly improves the accuracy and reproducibility of electrical characteristics of OFETs. The hole μ of pentacene OFET with an average 1 ML (~ 1.57 nm) thickness has been observed under a vacuum. The μ of pentacene OFET rapidly increases with increasing surface coverage in the region of film thickness less than saturation thickness (d_0), which is about 3.2 ML for pentacene OFETs studied herein. We have observed that pentacene molecular layers beyond d_0 have little contribution to the carrier transport in the semiconducting channel. The threshold voltage (V_T) of pentacene OFETs has a variable thickness dependence having minimum ~ 17 V at pentacene thickness around 3.2 ML. Similar d_0 was verified for both drain current and on/off current ratio of pentacene FETs. The atomic force microscopy (AFM) images of the pentacene layer confirm the layer-plus-island (Stranski-Krastanov mode) pentacene growth mechanism on SiO₂ substrate. Terrace-like stacking structure begins to be discernable around 3.2 ML of pentacene thin film. From AFM images, top few layers of pentacene terrace stacking become smaller in size after reaching the largest domain size around 10 ML. Our experimental results have demonstrated that the growth quality of the first few pentacene MLs on substrate strongly influences the morphology of the thicker film, packing structure, and electrical characteristics of OFET, including change-carrier mobility.

KEYWORDS: field-effect transistors • in situ measurement • thickness dependence • molecular monolayer • pentacene

INTRODUCTION

Organic field-effect transistors (OFETs) have received considerable interest in recent years because of their ease of fabrication, low-cost production, and mechanical flexibility (1). For organic semiconductor material pentacene, field-effect mobilities greater than 1 cm²/V s have been reported by many research groups (2). Pentacene thin film can be deposited by thermal vacuum evaporation as well as from solution processes (3), and it is one of the most promising candidate for industrial application. Dodabalapur et al. have fabricated OFETs using vacuum-sublimed α -hexathienylene (α -6T) thin films with different number of molecular monolayer (ML) and they have demonstrated that the field-induced conductivity in active layer occurs only near the interfacial plane (4). In fact, the effects of active layer thickness on OFET performance have been studied for a variety of organic semiconductor materials,

such as copperphthalocyanine (CuPc) (5), sexithienyl (6), pentacene (7), dihexylquaterthiophene (DT4T) (8), quaterylene (9), and poly (3-hexylthiophene) (10). Although operation models of OFET have been proposed, the saturation thickness (d_0) of the field-effect mobility of OFET is material dependent and it has determined by how many molecular layers are required to achieve the efficient transport properties. For example, recent studies by Ruiz et al. have shown that the d_0 of OFET is greater for pentacene than for α -6T (7). One may speculate that such different d_0 values are due to the charge trap with different magnitude at semiconductor/dielectric interface and the device fabrication/process dependent. Such a difference might explain that pentacene is more susceptible to interfacial charge traps than other organic semiconductors (11). The result confirmed that the current density of OFET may be sustained in just the first few MLs. The fundamental charge mobility of pentacene thin films depends on an optimal intermolecular π -orbital overlap, which in turn depends on the quality of molecular packing or ordering (12).

Focusing on organic semiconductor pentacene, Ruiz et al. and Yang et al. have determined d_0 of top-contact pentacene OFET around 6 ML and 15–20 nm (equivalent to 9.4–12.5 ML assuming 1 ML of pentacene has a thickness

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Received for review April 17, 2010 and accepted July 2, 2010

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DOI: 10.1021/am1003377

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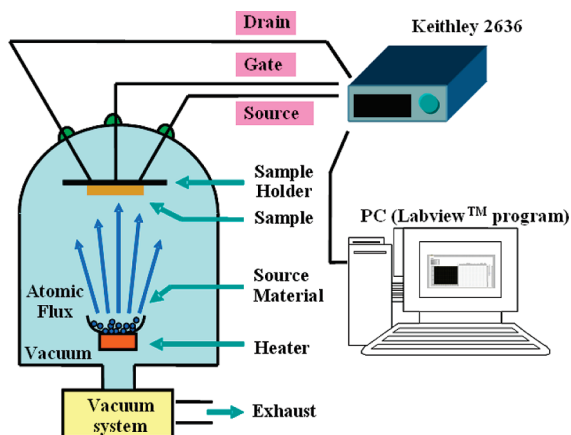


FIGURE 1. Schematic illustration of the thermal vacuum deposition of a pentacene thin film transistor (a bottom contact transistor) and its in situ electrical measurement setup with the vacuum chamber pressure around 6×10^{-6} Torr.

of 1.6 nm), respectively (7, 13). The discrepancy in d_0 values is mainly due to the different surface energy of different gate insulators. On the other hand, the discrepant d_0 values (4–6 nm) are still there in a relatively crude in situ characterization on bottom-contact pentacene OFETs by Kiguchi et al. (14) All these different results manifest that more reproducible data (without the disturbance from ambient atmosphere) (15) of the thickness dependence of OFET electrical properties should be retrieved again by a more comprehensive in situ characterization continuously under a high vacuum. Besides carrier mobility and current density, none has been addressed in the original report by Kiguchi et al. on the evolution of the other electrical characteristics (threshold voltage and on–off ratio) (14). More importantly, none of their data were reported with the correlation of pentacene surface morphology or molecular packing structure (14). Clarifying relationship between the electrical characteristics and molecular ordering of first few MLs is crucial in insightful understanding of the charge transport of OFET. In this paper, it is very appropriate and necessary to revisit the pentacene OFETs with continuous in situ characterizations to systematically study the pentacene growth mechanism and its relation to more comprehensive electrical characteristics of OFETs. We report the molecular packing and surface morphology of pentacene thin film by atomic force microscopy (AFM). The pentacene thin film is composed of multilayer of pentacene molecules grown by controlled thermal vacuum deposition, which was conducted by the laboratory-designed thermal vacuum deposition chamber equipped with the powerful in situ electrical characterization apparatus (Figure 1). Pentacene thin film transistors were fabricated layer-by-layer and electrically characterized continuously at the same time. A series of electrical measurement were performed on a same transistor (a bottom-contact OFET with different pentacene layer thickness) inside our chamber under high vacuum. In this fashion, we are able to have a precise calibration on the thickness dependence of carrier mobility (μ), threshold voltage (V_T), drain current, and OFET on/off

ratio. Insightful correlation between the thin film molecular packing and the OFET electrical characteristics can be delineated.

EXPERIMENTAL SECTION

The pentacene organic semiconductor was purchased from Aldrich. It was evaporated with a deposition rate of 0.4 ML/min (1 ML \approx 1.57 nm) in a home-assembled vacuum chamber (pressure below 6×10^{-6} Torr) internally equipped with electrical measurement apparatus (see Figure 1). The OFET electrical measurement was in situ carried out while the device remained inside the vacuum chamber under high vacuum condition. The pentacene deposition rate was probed by a quartz crystal monitor (QCM), which was calibrated by a surface profiler (Veeco Dektak 150) in advance. The fabricated OFETs are bottom contact device having variable pentacene thin film thickness from 1 to 20 MLs. During pentacene deposition, the substrate was kept constant at ambient temperature (\sim 300 K). The OFETs were built on top of heavily doped silicon substrates, which were covered with a thick layer (\sim 300 nm) of thermally grown SiO_2 ($C_i = 12 \text{ nF/cm}^2$). Here, Si wafer is the gate electrode and the oxide layer serves as the gate insulator. The Si wafer was ultrasonically cleaned in acetone and isopropanol, respectively, and it was then etched in dilute solution of sulfuric acid. Before the thermal vacuum deposition of pentacene, the SiO_2 -covered Si wafer substrates were patterned with source and drain electrodes made of gold contact layer (\sim 50 nm) by photolithography. The experiments were measured on devices with channel length of $10 \mu\text{m}$ and width of $2000 \mu\text{m}$, respectively.

The OFET electrical measurements were conducted by a semiconductor parameter analyzer (Keithley 2636), which has extended its electrical contact to OFET inside the vacuum chamber. The saturation mobility (μ_{sat}) was extracted from the slope of the square root of the drain current plot vs V_G from equation: 1

$$I_{D,\text{sat}} = \frac{W}{2L} C_i \mu_{\text{sat}} (V_G - V_T)^2 \quad (1)$$

where $I_{D,\text{sat}}$ is the drain-to-source saturated current; W/L is the channel width to length ratio; C_i is the capacitance of the insulator per unit area, and the V_G and V_T are gate voltage and threshold voltage, respectively.

In surface morphology characterization, organic thin films were deposited on SiO_2/Si wafers that were cleaned by sonication in acetone, methanol and deionized water. The surface morphology was examined by AFM (noncontact mode; Park system XE-100). The surface roughness (rms) of the cleaned SiO_2/Si wafer is 0.2 nm.

The surface energy of SiO_2 and pentacene was evaluated by measuring the contact angles of two test liquids, water and diiodomethane. Whereas the total surface energy (γ_s) is the sum of dispersion (γ_s^d) and polar (γ_s^p) components (16), eq 2 can be used to solve γ_s^d and γ_s^p of the surface energy.

$$1 + \cos \theta = \frac{2(\gamma_s^d)^{1/2}(\gamma_{lv}^d)^{1/2}}{\gamma_{lv}} + \frac{2(\gamma_s^p)^{1/2}(\gamma_{lv}^p)^{1/2}}{\gamma_{lv}} \quad (2)$$

The surface energy (γ_{lv}), the dispersion component (γ_{lv}^d), and the polar component (γ_{lv}^p) in this equation are 72.2, 22.0, and 52.2 mJ/cm² for water, and 50.8, 48.5, and 2.3 mJ/cm² for diiodomethane, respectively.

RESULTS AND DISCUSSION

Electrical Properties of Standard OFET. Figure 2a shows the typical drain current–drain voltage characteristics

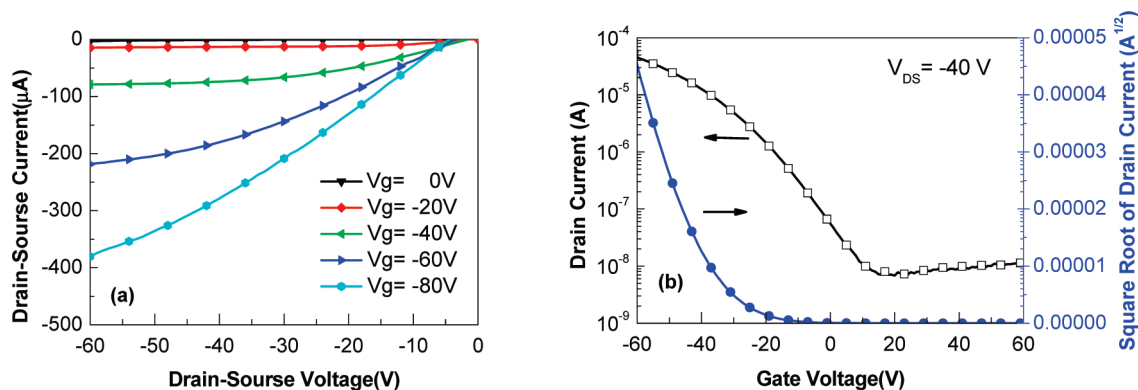


FIGURE 2. (a) Drain current–drain voltage and (b) drain current–gate voltage characteristics of 10 ML thick pentacene FET.

of a 10 MLs pentacene thin film transistor measured under high vacuum at room temperature. The negative gate voltages imply a hole-accumulated mode of the device. When increasing the drain voltage (V_D), both linear and saturation regions can be observed in the current–voltage plot as long as V_G being applied (> -20 V in our experiment). In bottom-contact OFET, the μ calculated in the saturation region is about $0.05 \text{ cm}^2/(\text{V s})$. The on–off ratio and V_T are extracted to be $>1 \times 10^4$ and -22 V (Figure 2b), respectively. Our determined μ value of the 10 MLs pentacene OFET is substantially higher than $\sim 0.03 \text{ cm}^2/(\text{V s})$, reported by Dimitrakopoulos et al. for the bottom-contact device at room temperature without thermal treatment or self-assembly monolayers (SAMs) modified gate insulator (17). Note that the carrier mobility is lower and off-current (drain current below 1×10^{-8} A at zero V_G) is higher than those of top-contact or SAM-modified bottom-contact device (2). This is attributed to the great dependence of OFET electrical characteristics on the molecular packing structure and the contact barrier at organic semiconductor/electrode interface (18). Because the contact resistance is one of the critical issues in optoelectronic device based on organic materials, the current injection at electrode/semiconductor interface has been widely investigated by several methods, such as four-probe measurement (19), the scanning probe potentiometry (20), and transmission line model (21). In addition, the molecular packing structure and morphology of the pentacene film on different electrode may influence the hole injection efficiency or contact barrier (22). In the present study, in order to simplify charge transporting issue of pentacene OFETs and to compare with data reported by Kiguchi et al., Au electrode is commonly employed as S/D electrodes to reduce the contact barrier because of its relatively high work function of ~ 5.1 eV, which is close to the HOMO energy level of pentacene (5.2 eV) (23). On the other hand, no hysteresis is found in all electrical characterizations, showing extremely low trap density at the interface of organic/insulator in OFET fabricated in this study. This is an indication of good reliability of our device fabrications and their electrical measurement.

Thickness Dependence of Carrier Mobility. We plotted the carrier mobility as a function of the thickness of pentacene films grown at room temperature by in situ electrical characterization (shown in Figure 3). The mobility

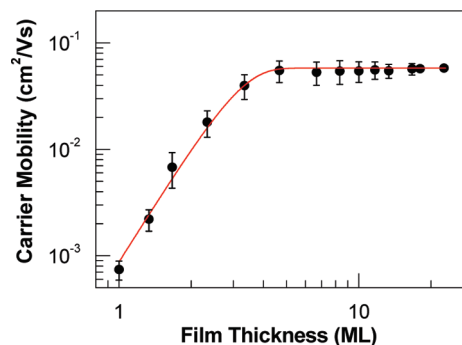


FIGURE 3. Charge-carrier mobility in the saturation regimes as a function of the thickness of the pentacene thin film. The red line is a fitting curve to eq 3.

value was deduced by using eq 1 and the error bars correspond to the highest and lowest mobilities (at least four devices were measured for each thickness). Following the analysis model of spatially correlated charge transport in organic thin film, the solid line in Figure 3 is fit to eq 3

$$\mu = \mu_{\text{sat}} \left(1 - \exp \left[- \left(\frac{d}{d_0} \right)^\alpha \right] \right) \quad (3)$$

where μ_{sat} , d , d_0 , and α are the saturated carrier mobility, film thickness, film thickness with saturated carrier mobility, and exponent, respectively. The exponent parameter α is the factor of carrier concentration from the interface of organic channel/insulator. Thus, these parameters indicate the degree of carrier localization in the conducting pathway. In Figure 3, the data points were extracted resulting $\mu_{\text{sat}} = 0.058 \pm 0.02 \text{ cm}^2/(\text{V s})$, $d_0 = 3.2 \pm 0.2$ ML, and $\alpha = 3.6$, respectively. Carrier mobility increased dramatically with the thickness: $0.0073 \text{ cm}^2/(\text{V s})$ at the early growth stage of 1.57 nm (~ 1 ML) and $0.058 \text{ cm}^2/(\text{V s})$ for films thicker than 34.5 nm (~ 23 ML). We have successfully observed the carrier mobility of pentacene OFET with average thin film thickness about 1 ML. On the other hand, our d_0 of 3.2 ML agree well with previously reported values because the deposition rate was very similar during the growth of thin film process (14). Both Pratontep et al. and Dinelli et al. have demonstrated that the deposition rate of organic semiconducting material is essential to the field-effect mobility of OFET (13, 24). Our d_0 of 3.2 ML also roughly agreed with the 4–6 nm (equiva-

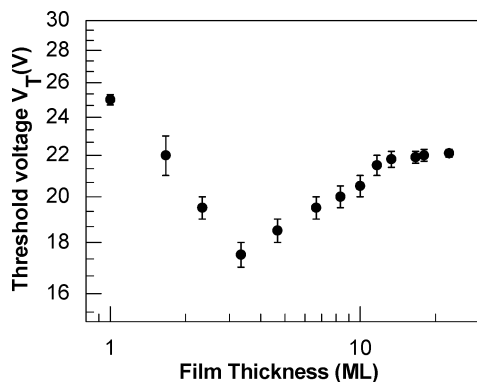


FIGURE 4. Dependence of V_T as a function of the thickness of the pentacene film.

lent to 2.5–3.75 ML assuming 1 ML corresponds to 1.6 nm reported by Kiguchi et al. (14) In this study, we have also found both d_0 and μ are highly correlated with the initial growth process of the pentacene thin film (see AFM analysis section).

We note that d_0 3.2 ML of pentacene is substantially greater than 1–2 ML of α -6T (4), 2.5 ML of DH4T (9), but lower than 6 ML of CuP c (5). However, it is quite similar to 3–4 ML found for quaterylene OFET (9, 25). One implication herein is the effective thickness of the transport layer in OFET depends on the molecular packing structure on the surface of the gate insulator. Our electrical characterization and surface morphology (which will be discussed later) have shown the surface coverage of pentacene is nearly complete at the thin film thickness around 3.2 ML. This estimated value is consistent with the observation that the charge carrier is localized in the first few MLs to the insulator–organic interface, where the film structure and morphology play an important role in device performances. We have found that the field-effect mobility requires only about 3.2 MLs or 5 nm in reaching saturation state of field-effect mobility; the contribution of charge carrier density is negligible beyond 3.2 MLs. We also infer our results to the improvement in the molecular packing structure (or interconnection of three-dimensional pentacene islands in thin film proposed and demonstrated by Yang, et al.) (13) in the first few MLs, which is essential for improving the carrier transport properties.

Thickness Dependence of Threshold Voltage. In addition to the charge-carrier mobility, the threshold voltage (V_T) is an important parameter that needs to be controlled to ensure proper operation of the circuits. It is well-known that the V_T value may depend on gate stress (26), exposure of environment (27), gate insulator material (28), and work function of source and drain electrodes (29). With powerful in situ electrical characterization, we are able to clearly show that there is a nonlinear thickness dependence of V_T in a bottom-contact pentacene OFET (Figure 4). Incidentally, the thickness having minimum V_T is accordant to the thickness of reaching saturation stage. The V_T is extracted in the saturation region (eq 1) at $V_{DS} = -40$ V by plotting $\sqrt{I_D}$ versus the gate bias V_G and extrapolating to zero current of I_D . When the active layer is very thin, i.e., less than 3.2 ML of d_0 , it is apparent that V_T increases almost linearly with the

decrease of film thickness. Horowitz et al. have reported that the charge carrier transport of ultrathin polycrystalline film is limited by the electric field across the interface of insulator and organic layer, flat band potentials, and fixed charges in the bulk material or interfacial surface (30). Accordingly, in the field-effect current unsaturated region, V_T is given by (31)

$$V_T = \frac{qp_0d_s}{C_i} + V_{FB} \quad (4)$$

where q is the charge of an electron, p_0 denotes the bulk hole density, V_{FB} means the flat-band potential of the organic layer, C_i is the capacitance of the insulator layer, and d_s is the thickness of organic layer. This can explain the apparent decrease of V_T with the film thickness less than d_0 (~ 3.2 ML). According to our data, p_0 and V_{FB} are calculated to be $1.53 \times 10^{18} \text{ cm}^{-3}$ and -27.66 V, respectively.

In contrast, when the active thin film layer is thicker, i.e., >3.2 ML of d_0 , the presence of a charge injection barrier from drain and source electrodes leads to an increase of V_T (32). This is due to the gold electrode having charge injection barrier up to 1 eV at the interface and the thick layers do not effectively increase the charge carrier density (33). This issue has been a major concern for organic electronics, where injection efficiency is one of the important factors of the device performance (34). Therefore, V_T linearly increases with the thickness of the active layer (see Figure 4) and the rise of V_T reaches the saturation stage -21 to -23 V, which are relatively higher than -17 V of minimum V_T . This is a direct physical evidence showing optimal thin film thickness is necessary for lowering V_T of OFET. It also explains why the optimal thickness is often found in a range of 5–40 nm for organic semiconducting materials (35, 36).

Thickness Dependence of Drain Current and on/off Ratio. Figure 5a shows the drain current of devices as a function of pentacene thickness at $V_G = V_{DS} = -80$ V. Increasing the film thickness toward ca. 3.2 ML, the drain current of the device increases rapidly. However, when the film thickness is thicker than saturation thickness of ca. 3.2 MLs, the magnitude of increasing drain current is significantly less than that ahead of 3.2 ML. The drain current of a thick film in OFET is limited by the charge carrier mobility of the bulk material, which is not necessary as ordered as thin films with just few MLs. Nevertheless, it is conceivable that the effective thin film thickness can extend beyond the initial few MLs in a well-ordered polycrystalline thick film.

The on/off ratio of drain current was estimated from the highest current and the lowest off current of OFET characteristics (such as the one shown in Figure 2b at drain voltage of -40 V). The thickness dependence of drain current on/off ratio is shown in Figure 5b. Because the off drain current remains nearly constant around 10^{-9} A, the fast increase of the drain current is the major cause for OFET with rising on/off ratio in the first few MLs. We would expect that the surface potential of the first few MLs remains relatively high, although it falls steadily with the accumulation of pentacene molecules (see discussion in the next section). For drain

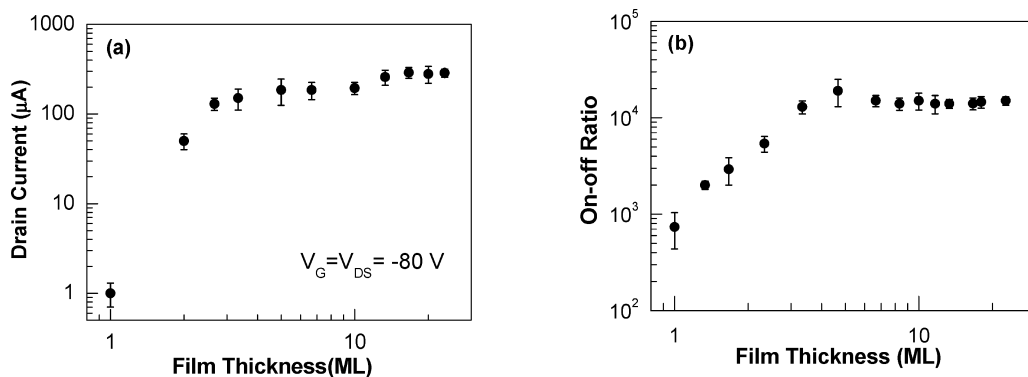


FIGURE 5. Dependence of (a) the drain current and (b) on-off ratio as a function of the thickness of the pentacene film.

current on/off ratio, the rising trend is leveling off when the film thickness beyond 3.2 ML in accord with the trend observed for drain current (Figure 5a). Once again, 3.2 ML seems to be the consistent optimal number similar to that found for μ (Figure 3) and V_T (Figure 4). This is also consistent with the fact that the top portion of a thick film of pentacene is more distance to the gate insulator and hence less susceptible in collecting charge carriers that are electric field-effective.

AFM Surface Morphology and Molecular Packing Structure Analyses. To understand the thickness dependence of the electrical characteristics of OFET, it is necessary to know the growth mechanism of pentacene thin film. In fact, the film morphology has been shown critically for charge carrier mobility (37–39). For thin film transistors, the morphology of the first few MLs is particularly important, where the density of state (DOS) of charge carrier at the interface of semiconductor/insulator is expected to strongly influence the carrier transport property (40, 41). Importantly, coverage of the first ML is decisive in the carrier mobility of OFETs, of which large voids in the first ML and the subsequent layer grown upon not fully covered first ML can limit the charge carrier transport. Figure 6 shows the AFM image and topographic profile of about 1 ML pentacene. The average height of 1 ML pentacene is 1.57 ± 0.10 nm, which is approximately the length of the long-axis of pentacene molecule. This result suggests that the ultrathin film is composed of nearly upright pentacene molecules on SiO_2 surface (42).

Figure 7 shows the AFM micrographs of pentacene thin films with various film thicknesses ranging from 0.3 to 100 ML on the thermally grown bare SiO_2/Si substrate. We can observe the evolution of electrical characteristics associated with the changes of thin film morphology. From the evolution of the thin film surface morphology shown in Figure 7, a Stranski–Krastanov mode can be inferred to the growth pattern of pentacene thin film as demonstrated by other research groups (41, 43). Stranski–Krastanov growth mode illustrates the different growth mechanism between the first few MLs of thin film and the rest portion of the thicker thin film. In looking for reasons behind the different growth mechanism, we have investigated the surface energy of bare SiO_2 gate insulator and its 3.2 ML pentacene covered surface, and they are quite different as ~ 53.9 mJ/m² and ~ 25.2 mJ/

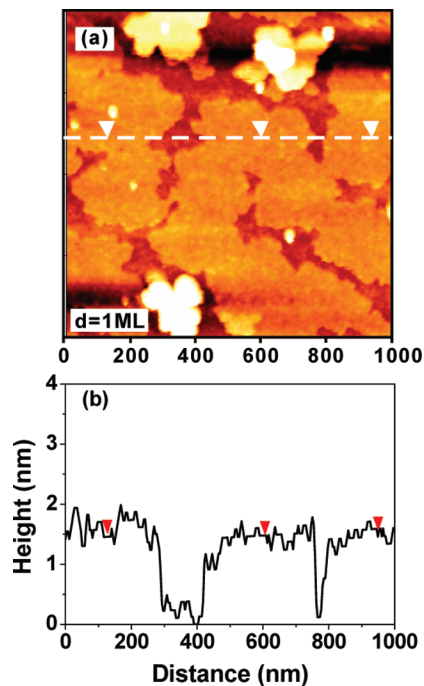


FIGURE 6. (a) Topographic profile of AFM image ($1 \times 1 \mu\text{m}$) of pentacene thin film with average 1 ML thickness, and (b) its scanning step profile following trace marked in panel a.

m², respectively. Previous studies indicate the control of the surface energy of the gate insulator can dominate the electrical characteristics of OFET by influencing the molecular packing structure of organic semiconductor (30). Accordingly, the interaction is stronger between SiO_2 gate insulator and pentacene molecules than among pentacene molecules themselves. Therefore, in the initial stage of thin film growth, the pentacene nuclei tend to grow laterally more than vertically to form local domain (see Figure 7a). At average 1 ML deposition stage, the incoming pentacene molecules are incorporated into the very thin layer with more surface coverage (see Figure 6 or Figure 7b). When the thickness reaches average 2 ML, a nearly full coverage of the first ML occurs in coexistence with large island-like patches of the second ML, sporadic third ML, and large voids in the layer (see Figure 7c). As more pentacene molecules are deposited further, terrace-like stacking domains start to form, although voids in previous layers are not completely filled (see Figure 7d,e). Presumably, there is a gradual change of growth direction from lateral to vertical direction. Viewing

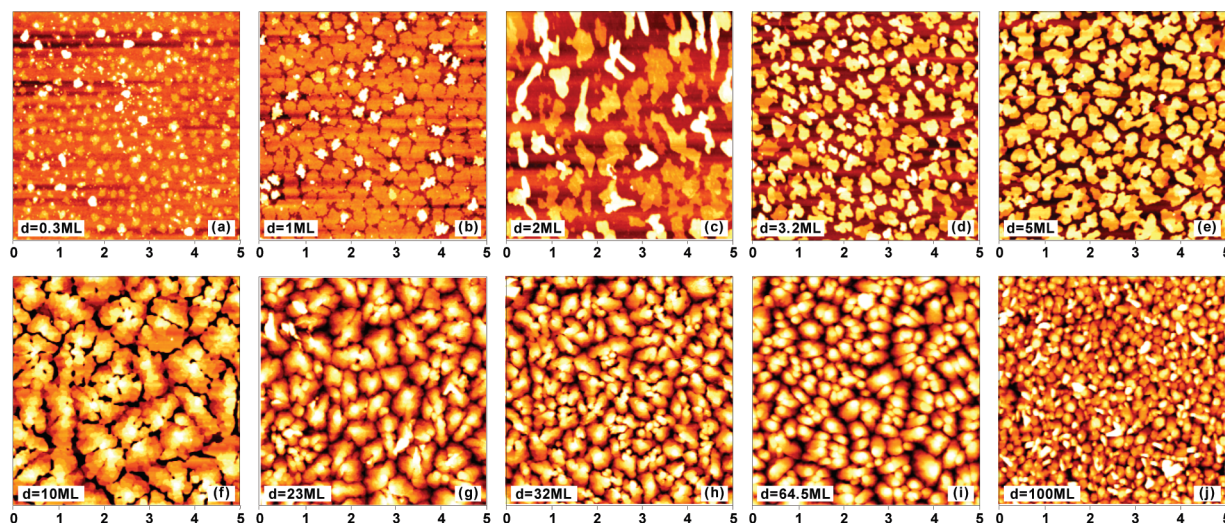


FIGURE 7. AFM images ($5 \times 5 \mu\text{m}^2$) of the surface of pentacene thin film (on SiO_2 substrates) with various thickness ranging from 0.3 to 100 MLs.

from AFM images, such transition of growth direction begins discernible around 3.2 ML growth stage, because the progressive formation of the terrace-like AFM image shown in Figure 7 is discernible around 3.2 ML and beyond. Referring to our surface energy estimation, the layer-by-layer gradual change of growth direction taking place in the first few MLs can be attributed to the drastic surface energy difference between SiO_2 gate insulator and pentacene thin film. At about 10 ML, terracelike features become very prominent in AFM surface image and reach most expanded domain size of each terrace stack (see Figure 7f). Such morphological feature can be persistently observed in the higher ML growth stages (see Figure 7g–j), but the domain size of the top few terraces is reduced continuously.

It is worth noting that pentacene thin film morphology shown in Figure 7f or 7g (10 or 23 ML growth stage in the present study) is often considered the optimal one for OFET's electrical performance. From our in situ electrical characterization shown above, we have demonstrated that such morphology (or the number of ML) may be good for μ , on–off ratio, and drain current, but is not ideal for low V_T of pentacene OFETs. Nevertheless, AFM images are consistent with what we deduce from the thickness dependence of electrical characterization, i.e., additional layers beyond the saturation thickness do not contribute efficiently to carrier percolation pathway and hence the field-effect mobility, reduced threshold voltage, drain current density, and on/off ratio of OFETs.

The AFM results suggest that the growth pattern hinges on a delicate balance of the anisotropic interaction among organic semiconducting molecules, molecular material and gate insulator material, which is also sensitive to the SAM surface modification or thermal treatment (41). Therefore, the exact d_0 value is material dependent and device fabrication/process dependent as well. For optimization of OFET performance concerns, the thickness dependence of OFET characteristics should be carefully examined by the powerful in situ electrical characterization, such as the one demon-

strated in this paper, for each potential organic semiconducting material.

CONCLUSIONS

In summary, we present the powerful in situ electrical characterization in determining the electrical saturation thickness and change carrier transport property in pentacene OFET. The electrical saturation thickness of 3.2 ML was determined for pentacene semiconducting thin film. Pentacene grown on SiO_2 gate insulator with a surface energy of 53.8 mJ/cm^2 was dominated by the Stranski–Krastanov growth mode, consistent with the lateral growth in the first few ML and terrace-like growth in higher MLs examined by AFM. In addition, AFM reveals the first pentacene ML with substantial voids space and the incomplete layer coverage on top of the first ML, which limits the transport channel and impairs the field-effect mobility and other electrical characteristics of OFET. Our study has demonstrated that pentacene semiconducting thin film in its optimal thickness can promote its OFET electrical performance.

Acknowledgment. The authors thank Academia Sinica and National Science Council (Grants NSC 98-2119-M-001-026 and 97-2628-M-001-014-MY3) of Taiwan for financial support.

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AM1003377